[0107] The shape of the cross section of bottom electrode **65** (shape of etched polycrystalline silicon film **600** in FIG. 6G) can be controlled depending on the dry etching condition. For example, if bottom electrode **65** has a tapered shape (shape of bottom electrode **65** having the area of the bottom surface larger than that of the top surface), interlayer insulation film **70** can be readily embedded between gate electrode **60** and bottom electrode **65** to attain good insulation therebetween. Conversely if bottom electrode **65** has an inverted tapered shape (shape of bottom electrode **65** having the area of the top surface larger than that of the bottom surface), emitter electrode **90** and bottom electrode **65** can have a large contact area therebetween to reduce the contact resistance.

OTHER EMBODIMENTS

[0108] Although one embodiment according to the present invention has been described above, it should not be understood that the description and the drawing included as part of this disclosure are limitation to the invention. Various alternative embodiments, examples, and techniques for implementation will be apparent to persons skilled in the art.

[0109] For example, a modification of the structure of gate electrode **60** in semiconductor device **1** is illustrated in FIG. **15** in which the bottom portion of gate electrode **60** is projected toward the central portion of groove **25** across the bottom surface of groove **25**. In FIG. **15**, the gap between gate electrode **60** and bottom electrode **65** is expressed as D, and the amount of the bottom portion of gate electrode **60** projected toward bottom electrode **65** in groove **25** is expressed as X. In this modification, the sum of the projection amount X and width d2 of bottom electrode **65** is preferably larger than gap W**2** between grooves **25**. In such a configuration, holes relatively readily concentrate on the regions under gate electrode **60** and bottom electrode **65** and drift region **20** near gate electrode **60** and bottom electrode **65**. Thereby further conductivity modulation specific to IGBTs can be generated to reduce on-resistance.

[0110] For example, larger gap D results in a reduction in the width of the depletion layer, which is formed under gate electrode **60**, on the side of bottom electrode **65**, reducing the breakdown voltage between emitter electrode **90** and collector electrode **80**. For this reason, the breakdown voltage can be controlled by gap D between gate electrode **60** and bottom electrode **65**.

[0111] A larger projection amount X of gate electrode **60** increases reverse transfer capacitance Crss. For this reason, reverse transfer capacitance Crss can be adjusted by projection amount X.

[0112] In the structure and the production method above, gap D and projection amount X can be determined by the mask patterns for photoresist film **200** and sacrificial oxide film **650** used in the gate electrode patterning step. For example, for protection of the semiconductor device, gap D and projection amount X can be determined such that the breakdown between emitter electrode **90** and collector electrode **80** occurs in a specific region of the chip. For example, a mask pattern having large gap D in this specific region can be used to readily reduce the breakdown voltage in the active region on the chip. In contrast, small gap D can reduce reverse transfer capacitance Crss. Namely, the distribution of the breakdown voltage or reverse transfer capacitance Crss in the plane of the chip can be controlled only by the mask pattern in lithography performed in the gate electrode patterning step. In lithography illustrated in FIG. 6F, light for exposure can be focused onto the bottom surface of groove **25** to control gap D and projection amount X with high precision.

[0113] As illustrated in FIG. **15**, the ratio of the sum of width d2 of bottom electrode **65** inside groove **25** and projection amount X to gap W2 between grooves **25** is preferably about ¼ to 1¼. At a ratio of less than ¼, holes are barely accumulated in drift region **20**. In contrast, at a ratio of more than 1¼, channel resistance increases, and in turn on-resistance does.

[0114] In addition, to enhance the effect of accumulating holes by bottom electrode **65** and groove **25**, width d2 of bottom electrode **65**, projection amount X and gap W**2** between grooves **25** preferably satisfy the relationship expressed by the expression (d**2**+X)>W**2**. In particular, the relationship is preferred in semiconductor device **1** having high breakdown voltage.

[0115] Alternatively, emitter region **40** may be formed such that the first portion on the top surface side of semiconductor substrate **100** has an impurity concentration of 1E19 atom/cm^3 to 1E20 atom/cm^3 and the second portion arranged at a deeper level than the first portion has an impurity concentration of 1E18 atom/cm^3 to 1E19 atom/cm^3. Such a configuration can attain semiconductor device **1** having a high short-circuit capacity.

[0116] Semiconductor device **1** in FIG. **1** has groove **25** with a flat bottom. Groove **25** may be formed to have a bottom such that the central portion of groove **25** is shallower than the end of groove **25**. Groove **25** having such a bottom can accumulate holes in the central portion of the bottom of groove **25** more efficiently. As a result, on-voltage can be reduced.

[0117] Alternatively, at least part of the bottom of groove **25** may have a curved surface projected downward. If the bottom of groove **25** has an end with a large curve, holes readily move to base region **30** without being accumulated under groove **25**. For this reason, groove **25** having a large flat bottom or a large projection on the bottom can reduce on-voltage.

[0118] FIG. **13** illustrates a sectional view of the connection portion between groove **25** and connection groove **125**. Emitter electrode **90** is connected to bottom electrode (bottom electrode body) **65** via connection portion **301** to bottom electrode **65**, which is opening **301** arranged in interlayer insulation film **70**. Connection portion **301** is arranged at the end in the extending direction of bottom electrode **65**, and is located at or outside of the end of the region in which left and right gate electrodes **60** face each other. In short, connection portion **301** is arranged outside of the active region. For example, formation of connection portion **301** generates a narrow recess on the top surface of emitter electrode **90** above connection portion **301**, which is arranged in the active region. Such a recess reduces the connection strength between emitter electrode **90** in the active region and the bonding wire. Accordingly, bottom electrode **65** is preferably connected to emitter electrode **90** only at the end of bottom electrode **65** spaced from the active region. Furthermore, formation of connection portion **301** may lead to unintentional invasion of moisture content into groove **25**. The invasion of moisture content into the active region reduces reliability of the semiconductor device significantly. Connection portion **301** is preferably formed only at the end of bottom electrode **65**, that is, in the outer peripheral region. As illustrated in FIG. **13**, base region **30** may be formed to the outside region of connection groove **125**. Such a configuration can